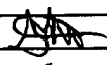
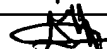


#4

Form PTO-1449 (Modified)	File Dock t No.: 042390.P9001	Serial No.: 042390 Y t Assigned
List of Patents and Publications Statement (Use several sheets if necessary)		Applicant: Bharat, Bhushan, et al.
Page 1 of 3		Filing Date: H rewith

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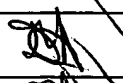


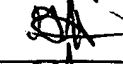

12/17/01

REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials		Document No.		Class	Sub-Class	Filing date if appropriate
	AA	5,341,322	Fettweis, et al.	364	764	5/11/92
	AB	5,270,962	Fettweis	364	766	3/11/93
	AC	4,890,127	Darley	364	786	12/26/89
	AD	5,115,408	Darley, et al.	364	754	2/5/91
	AE	5,923,579	Widigen, et al.	364	786.01	2/22/95
	AF	5,418,736	Widigen, et al.	364	786	3/11/94
	AG	5,815,420	Steiss	364	736.04	7/31/97
	AH	5,206,825	Takagi, et al.	364	746.2	3/24/92
	AI	4,422,143	Guttag	364	200	11/24/80
	AJ	5,696,954	Guttag, et al.	395	562	6/7/95
	AK	3,935,438	Grupe	235	174	10/11/74
	AL	4,709,226	Christopher	340	347DD	7/15/85
	AM	5,808,928	Miyoshi	364	760.01	6/5/97
	AN	5,680,339	Moyse, et al.	364	745	6/7/95
	AO	4,972,362	Elkind, et al.	364	760	6/17/88
	AP	5,386,377	McClure	364	787	9/16/93
	AQ	5,144,577	Linnenberg	364	769	2/27/91
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	AT	4,967,388	Tate	364	760	4/21/88

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No.		Document No.	Date	Country	Class	Sub-Class	Translation
	AU						
	AV						

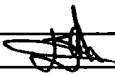
OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	PCT International Search Report, Application No. PCT/US 00/ 42165, date of completion of the search, July 3, 2001
	AX	Cortadella J. et al.: "Evaluation of A + B = K Conditions Without Carry Propagation" IEEE Transactions on Computers, Vol. 41, No. 11, November 1992
	AY	Parhami, B.: "Comments on Evaluation of A + B = K Conditions Without Carry Propagation" IEEE Transactions on Computers, Vol. 43, No. 4, April 1994
	AZ	Duprat J. et al.: "Ecrire les nombres autrement pour calculer plus vite" Technique et Science Informatiques, Vol. 10, No. 3, 1991
	BA	Parhami, B.: "On the Implementation of Arithmetic Support Functions for Generalized Sign-Digit Number Systems" IEEE Transactions on Computers, Vol. 42, No. 3, March 1993






Examiner D. H. Malzahn Date Considered 2/11/04

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Form PTO-1449 (Modified)		Priority Document No.: 042390.P9001		Serial No.: Not Yet Assigned			
List of Patents and Publications Statement (Use several sheets if necessary) Page 2 of 3				Applicant: Bharat, Bhushan, et al.			
				Filing Date: Herewith			

REFERENCE DESIGNATION			U.S. PATENT DOCUMENTS			
Examiner Initials	Document No.	Document No.	U.S. Patent Documents	Class	Sub-Class	Filing date if appropriate
	AA	5,754,819	Lynch et al.	395	421.08	7/28/94
	AB					
	AC					
	AD					
	AE					
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No.	Document No.	Date	Country	Class	Sub-Class	Translation	
	AU						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)		
	AW	Lutz, D. et al.: "Early Zero Detection", International Conference on Computer Design, pp. 545-550, 1996
	AX	Lutz, D. et al.: "The Half-Adder Form and Early Branch Condition Resolution" Arithmetic 13, pp. 266-273, 1997
	AY	Lutz, D. et al.: "Comparison of two's complement numbers" Int. J. Electronics, Vol. 80, No. 4, pp. 513-523, 1996
	AZ	Lutz, D. et al.: "Programmable Modulo-K Counters" IEEE Transactions on Circuits and Systems—I: Fundamental Theory and Applications, Vol. 43, No. 11, November 1996
	BA	Obaidat M. S. et al.: "Fast multi-step addition algorithm" Int. J. Electronics, Vol. 70, No. 5, pp. 839-849, 1991

Examiner: D.H. Malzahn	Date Considered: 2/11/04
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EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-1449 (Modified)

Atty Dock t No.:
042390.P9001

Serial No.: Not Yet Assigned

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Page 3 of 3

Applicant: Bharat, Bhushan, et al.

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
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No.		Document No.	Date	Country	Class	Sub-Class	Translation
	AU						
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OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Ling, H., "High-Speed Binary Adder", IBM Journal of Research and Development, Vol. 25, No. 2-3, pp. 156-166, May-June 1981
	AX	
	AY	
	AZ	
	BA	

Examiner

D H. Mulzahn

Date Considered

2/11/04

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Substitute for Form 1449A-PTO (Modified) (use as many sheets as necessary)		#5	Attorney Docket No.: 42390.P9001	Application Number: 10/032,026
Page 1 of 1			First Named Inventor: Bharat Bhushan, et al.	Examiner: Unassigned
			Filing Date: December 17, 2001	Art Unit: 2121 2124

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
1		4,569,032		Lee	02-04-1986	
2		4,858,168		Hwang	08-15-1989	
3		4,899,305		Needles	02-06-1990	
4		5,140,546		Ishikawa et al.	08-18-1992	
5		5,719,803		Naffziger	02-17-1998	
6		5,208,490		Yetter	05-04-1993	
7		5,285,406		Lynch et al.	02-08-1994	
8		5,329,477		Kudou	07-12-1994	
9		5,392,423		Yetter	02-21-1995	
10		5,581,497		Kumar	12-03-1996	

OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
1		Dobberpuhl, D.W., et al., "A 200-Mhz 64b Dual-Issue CMOS Microprocessor," IEEE Journal of Solid State Circuits, Vol. 27, No.11, November 1992, pp. 1555-1567.	
2		Inoue, A., et al., "A 0.4μ m 1.4ns 32b Dynamic Adder using Non-precharge Multiplexers and Reduced Precharge Voltage Technique," Symposium on VLSI Circuits Digest of Technical Papers, June 1995, pp. 9-10.	
3		Ling, H., "High-Speed Binary Parallel Adder," IEEE Transactions on Electronic Computers, vol. 15, October 1966, pp. 799-802.	
4		Naffziger, S., "A Sub-Nanosecond 0.5μm 64b Adder Design," ISSCC Digest of Technical Papers, 1996, pp. 362-363.	
5		Quach, N. et al., "High Speed Addition in CMOS," Stanford University Technical Report: CSL-TR-90-415, February 1990, 16 pgs.	
6		Suzuki, M., et al., "A 1.5-ns 32-b CMOS ALU in Double Pass- Transistor Logic," IEEE Journal of Solid State Circuits, Vol. 28, No.11, November 1993, pp. 1145-1151.	

Examiner Signature	D.H. Malzahn	Date Considered	2/11/04
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¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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